ELE 448 Lab 5
Due by 18 March, 2019

1. Finish Lab 4
   a. XOR
      i. schematic, simulation, and layout
   b. Negative Level D-Latch
      i. Schematic, simulation, and layout
   c. Positive Level D-Latch
      i. Schematic, simulation, and layout
   d. Positive Level D-Latch with Reset
      i. Schematic, simulation, and layout

2. XNOR; Please refer to the XOR from (1). The XOR can be made into an XNOR by adding an inverter; however, one can invert the operation by:
   a. Copy XOR-> XNOR
   b. Find a way, using the same architecture (2 inverters, & the 2 pass transistors) to implement the XNOR function; verify that it functions properly
   c. Carry the adjustment(s) into the layout; verify the layout, e.g. DRC & LVS

3. SR Latch; using the 2 input NAND that you created for the previous layout lab, implement an SR latch (synthesized from 2 NAND gates)
   a. Open the schematic editor; wire the SR latch (also create the symbol)
   b. Verify the schematic via simulation
   c. Generate the layout; verify the layout, e.g. DRC & LVS

Note:

- One can find drawings of this latch in chapter 5 of the textbook
- The SR Latch will have the following truth table

S	R	Q	$\overline{Q}$
1	1	Q	$\overline{Q}$
0	1	1	0
1	0	0	1
0	0	1	1

4. Draw a CMOS transmission gate (layout only)

Note:

- Information on transmission gates can be found in section 7.3 of the textbook

<u>Lab Write-up:</u>

For all components:

a. Schematic
   i. Provide an image
   ii. How many of each type of MOSFET were used in your design?
   iii. How does the component work?
b. Simulation
   i. Provide images
      1. Simulation setup and results
   ii. Does the output make sense?
      1. Provide a truth table
c. Layout
   i. Show an image of your layout
   ii. Explain how the device is represented in the layout
      1. Where is each component located?
   iii. Did DRC and LVS pass?
      1. If it failed, what did you have to modify to get them to pass?